Only for Autonomous
As prepared on: 05-03-2024

Progressive Education Society's

Modern College of Arts, Science and Commerce (*Autonomous*)

Shivajinagar, Pune -5

Time Table for Third Year UG

SCIENCE FACULTY

(T.Y.B.SC. ELECTRONIC SCIENCE) SEM V

CIE Backlog Examination, Mar-Apr 2024

(Sem-V Backlog)

Date	Time	Subject Code	Subject
22-03-2024	1.15 pm to 2.00 pm	19ScEleU501	Analog Integrated Circuits and applications
23-03-2024	1.15 pm to 2.00 pm	19ScEleU502	8051 Microcontroller interfacing and Applications
26-03-2024	1.15 pm to 2.00 pm	19ScEleU503	Digital System Design with Verilog
27-03-2024	1.15 pm to 2.00 pm	19ScEleU504	Principles of Semiconductor Devices
28-03-2024	1.15 pm to 2.00 pm	19ScEleU505	Fundamentals of Electronic Communication
30-03-2024	1.15 pm to 2.00 pm	19ScEleU506	"C" Programming

Dr. R. M. Jagtap
Controller of Examinations

Dr. Anjali Sardesai
Coordinator, IQAC

Dr. R. S. Zunjarrao
Principal

Instructions to Students:

1. The examination hall for CIE Backlog Examination will be communicated to you by concerned Department.
2. For any query related to CIE Backlog Examination time-table, please contact concerned subject teacher /Department.
3. For CIE Backlog Examination, please ensure that you will reach the examination Hall 10 minutes before examination time.
4. Duly signed Hall ticket and college ID card is compulsory to attend the examinations.
5. Use of mobile phone and smart watch is strictly prohibited.
6. If any misconduct by any student will be confirmed by Examination Squad during examination, then appropriate 'Disciplinary Action' will be admissible against the student as per SPPU rules.